Extra Practice Questions (SOLUTIONS)

NOTE THAT THERE ARE MANY OTHER POSSIBLE SOLUTIONS TOO…

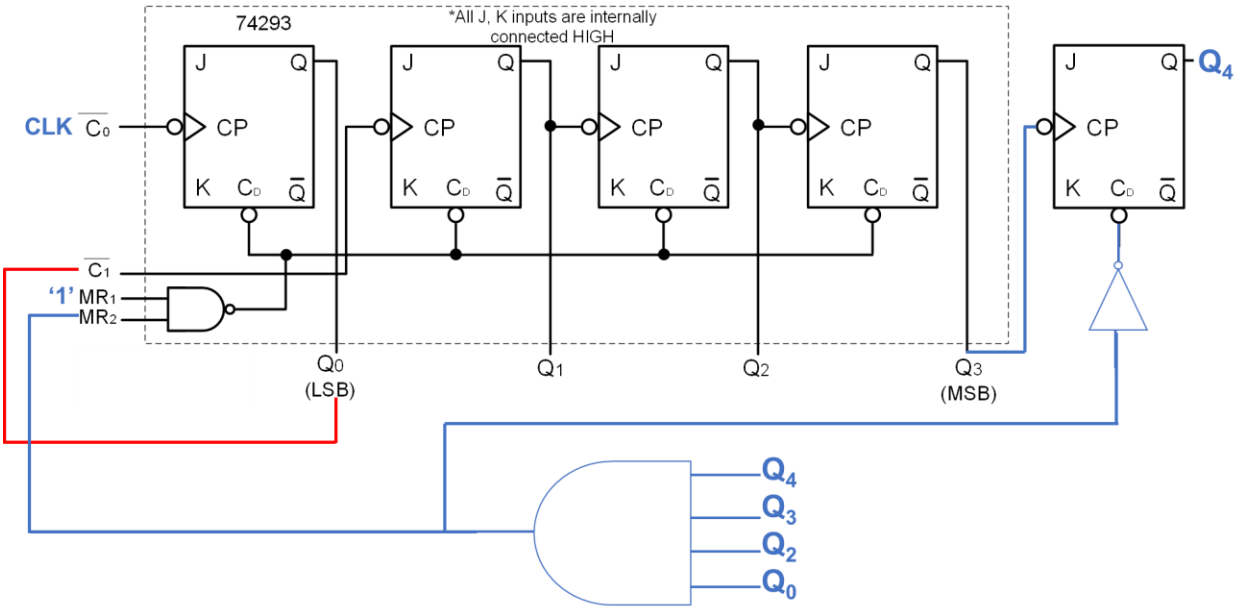
Question 1

We need an extra JK flip-flop to implement a 5-bit counter. For an ***asynchronous*** Mod-29 counter, it needs to be cleared asynchronously (immediately) when count reaches 29:

$Q_4\ Q_3\ Q_2\ Q_1\ Q_0$

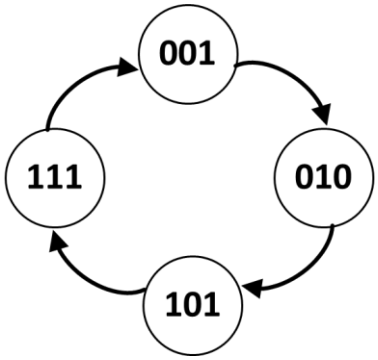
$29_{10} = (1\ \ 1\ \ 1\ \ 0\ \ 1)_2$

Since "11111" will not be reached for a mod-29 counter, the condition to be checked for is "111X1" i.e., we only need to detect $Q_4 = Q_3 = Q_2 = Q_0 = 1$ to clear the counter.

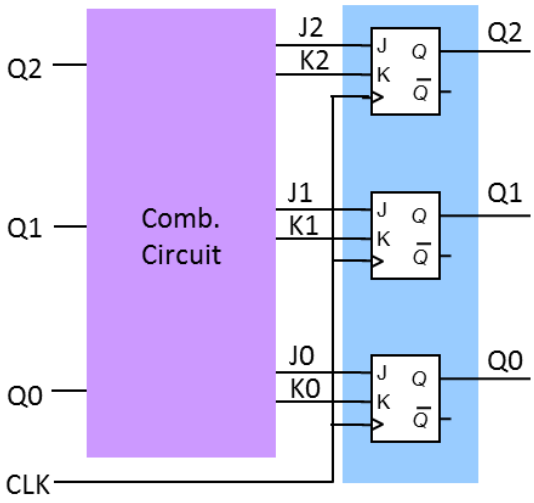


Question 2

1) State Diagram



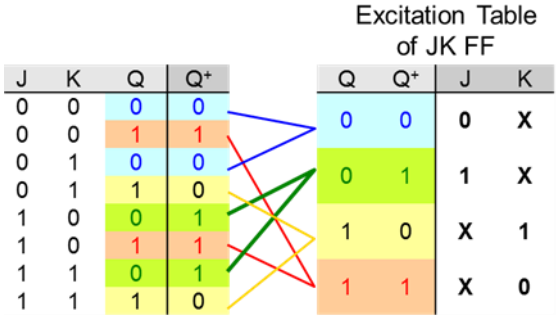
2) Functional Block Diagram



3) Next State Table

Current State			Next State		
Q2	**Q1**	**Q0**	**Q2+**	**Q1+**	**Q0+**
0	0	1	0	1	0
0	1	0	1	0	1
1	0	1	1	1	1
1	1	1	0	0	1
Other States			X	X	X

4) Apply Excitation Table to determine Output Values of Combinational Circuit



Q2	Q2+	J2	K2
0	0	0	X
0	1	1	X
1	1	X	0
1	0	X	1

Q1	Q1+	J1	K1
0	1	1	X
1	0	X	1
0	1	1	X
1	0	X	1

Q0	Q0+	J0	K0
1	0	X	1
0	1	1	X
1	1	X	0
1	1	X	0

5) Construct the truth table of the Combinational Circuit

Inputs of Comb. Ckt			Outputs of Comb. Ckt					
Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	1	0	X	1	X	X	1
0	1	0	1	X	X	1	1	X
1	0	1	X	0	1	X	X	0
1	1	1	X	1	X	1	X	0
Other States			X	X	X	X	X	X

6) Realize the Circuit

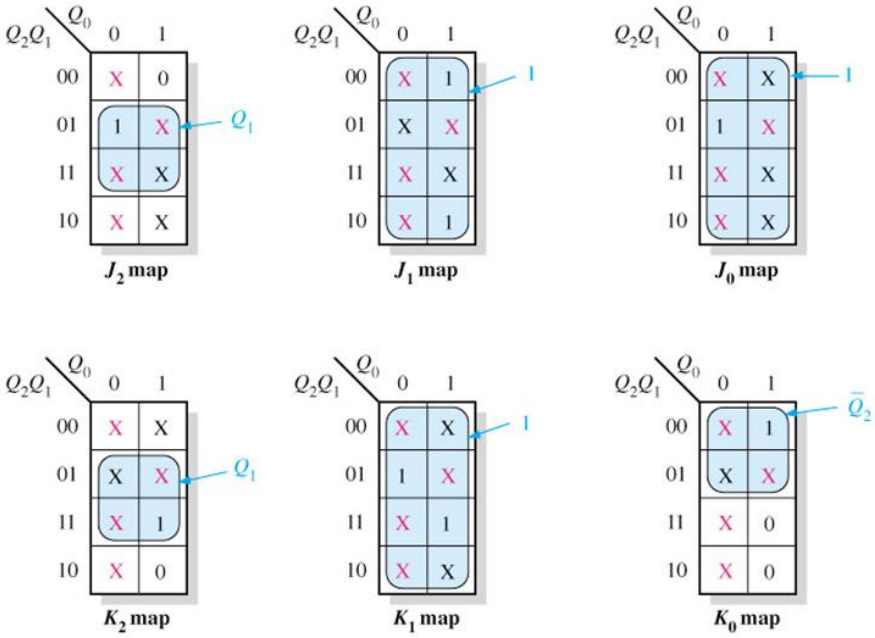
Method 1 : By inspection

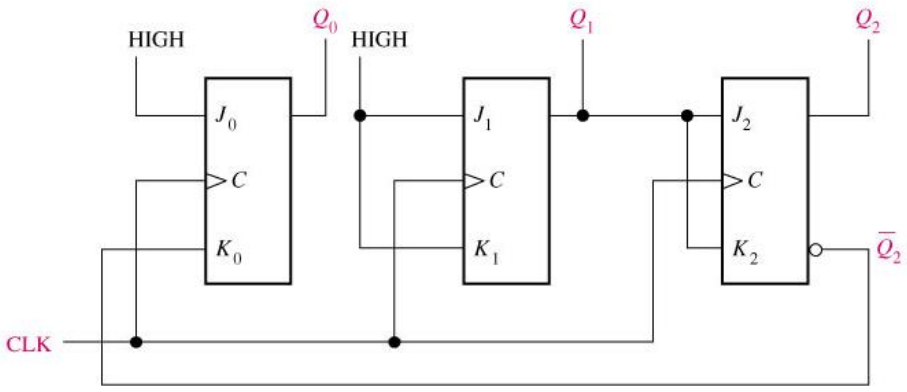
J2 = K2 = Q1 or $\overline{Q_0}$

J1 = K1 = 1

J0 = 1, K0 = $\overline{Q_2}$

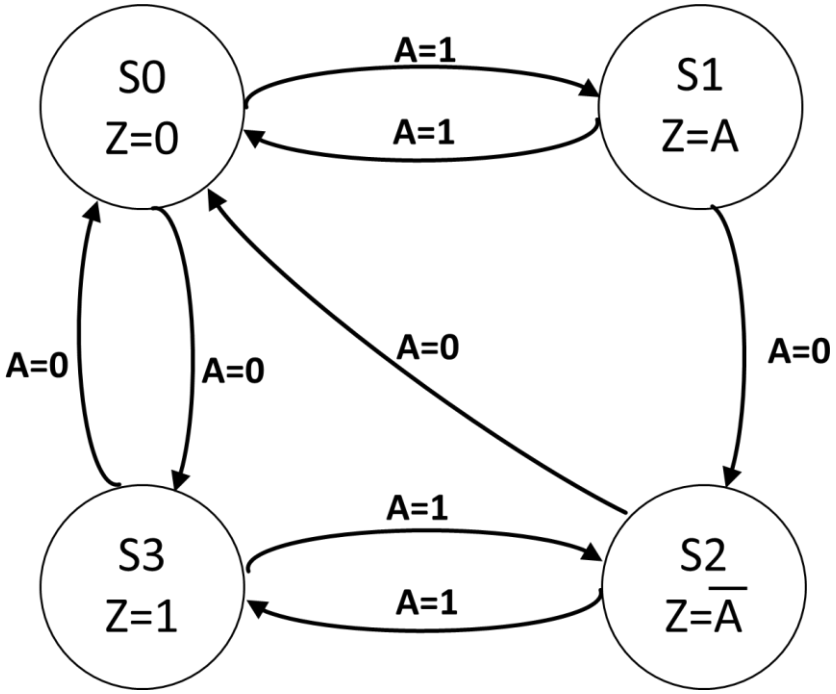
Method 2 : By KMAP





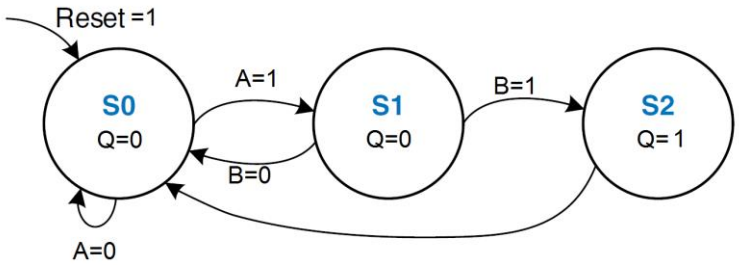
(ii) If the counter gets into state 3 ($Q_2Q_1Q_0$=011), based on the circuit above, the next count is $Q_2Q_1Q_0$=100, followed by 111. Thus, the counter will return to a valid state through 3 → 4 → 7.

Question 3



Possible state after two clock cycles : S0 or S3.

Question 4



Description:

This finite state machine asserts (sets TRUE) the output Q for one clock cycle if A is TRUE (‘1’) followed by B being TRUE (‘1’) in the next clock cycle. Otherwise, the machine deasserts the output Q (sets FALSE).

1) Next State Table

current state		inputs		next state	
s_1	s_0	a	b	s'_1	s'_0
0	0	0	X	0	0
0	0	1	X	0	1
0	1	X	0	0	0
0	1	X	1	1	0
1	0	X	X	0	0

$$S_1^+ = S_0 B$$

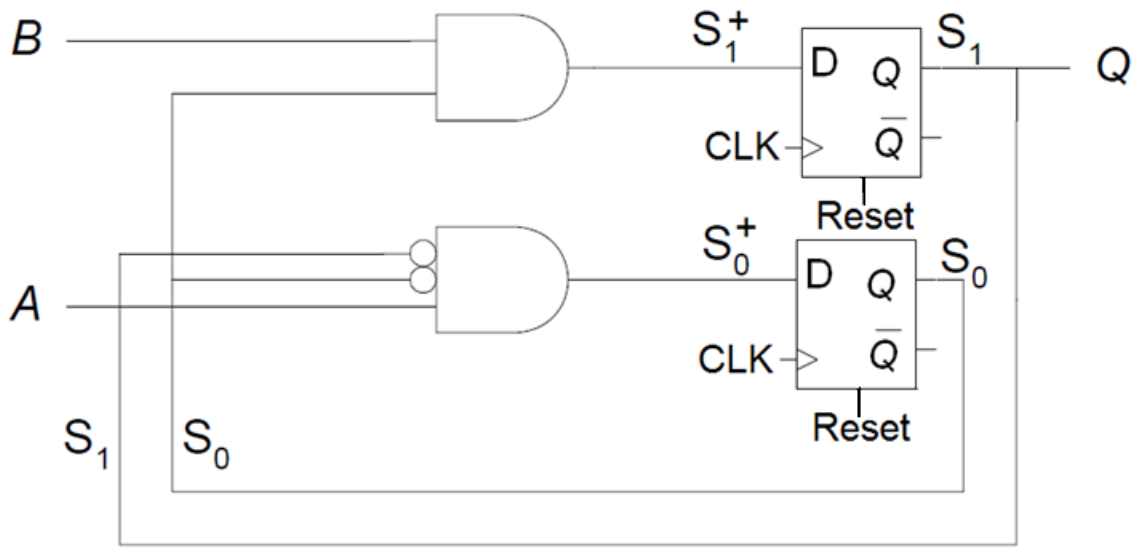
$$S_0^+ = \overline{S_1}\,\overline{S_0} A$$

2) Output Logic Table

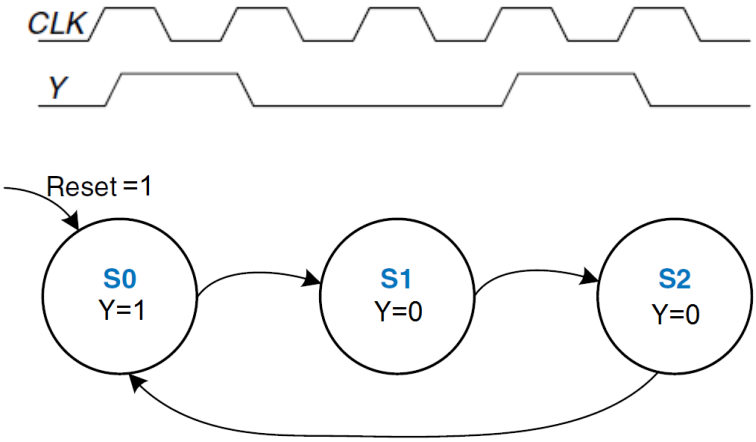
current state		output
s_1	s_0	q
0	0	0
0	1	0
1	0	1

$$Q = S_1$$

Using D-FFs with synchronous resets, the circuit is as follows :



Question 5



1) Using the following State Assignments :

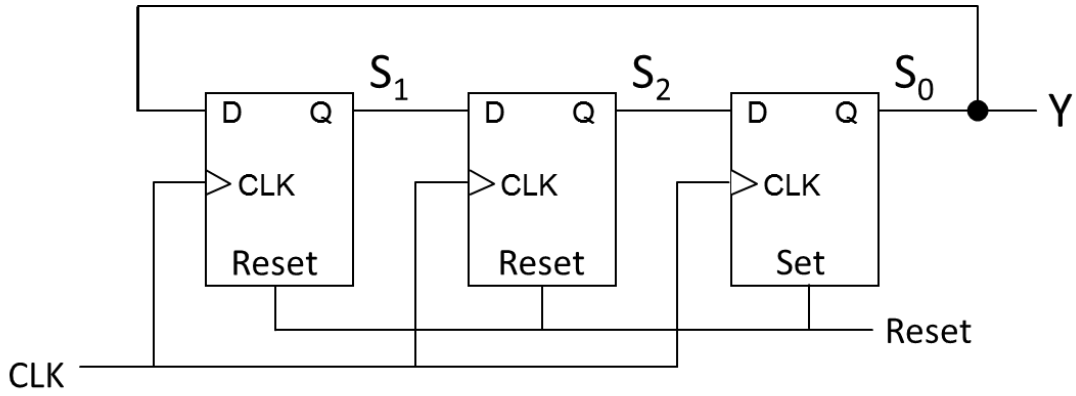
State	Binary Encoding S_2	S_1	S_0
S0	0	0	1
S1	0	1	0
S2	1	0	0

2) Next State Table

Current State S_2	S_1	S_0	Next State S'_2	S'_1	S'_0
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	0	0	1

$S_2' = S_1$, $S_2' = S_0$, $S_0' = S_2$, $Y = S_0$

Using D-FFs with active high synchronous resets and sets, the circuit is as follows :



Question 6

By working backwards from the circuit provided, the next state table can be derived as follows:

Next State Table

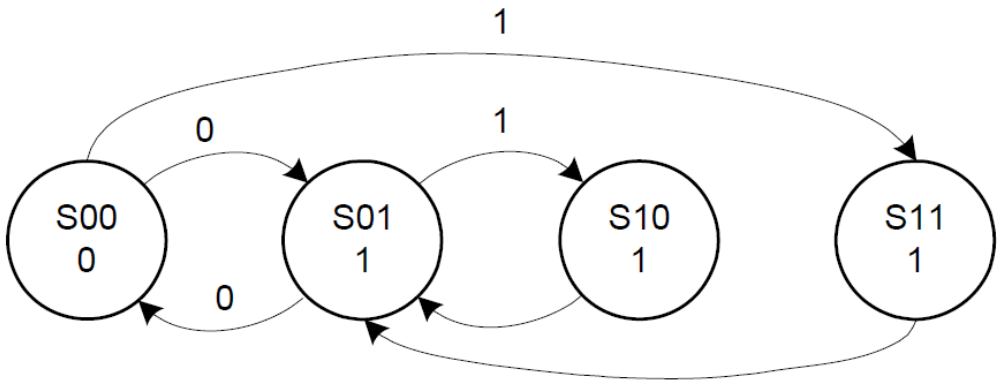
current state		input	next state	
s_1	s_0	x	s'_1	s'_0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	X	X	0	1

(Detailed working on subsequent pages)

Output Logic Table

current state		output
s_1	s_0	q
0	0	0
0	1	1
1	X	1

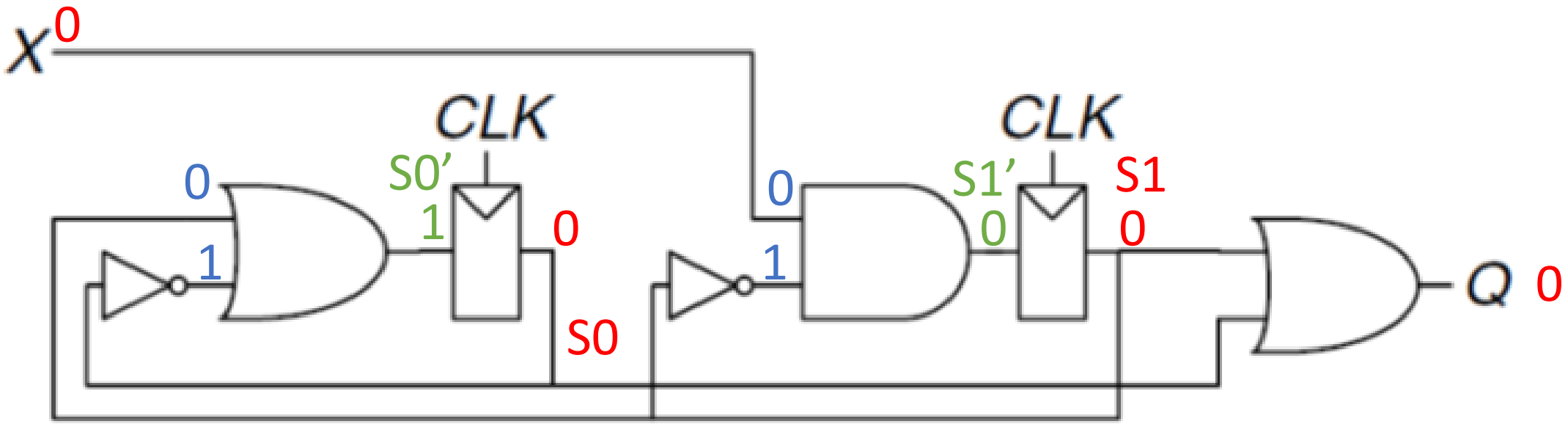
State Transition Diagram



This is a Moore machine.

When X = 1, this finite state machine is a divide-by-two pulse generator. When X = 1, the output Q is asserted HIGH.

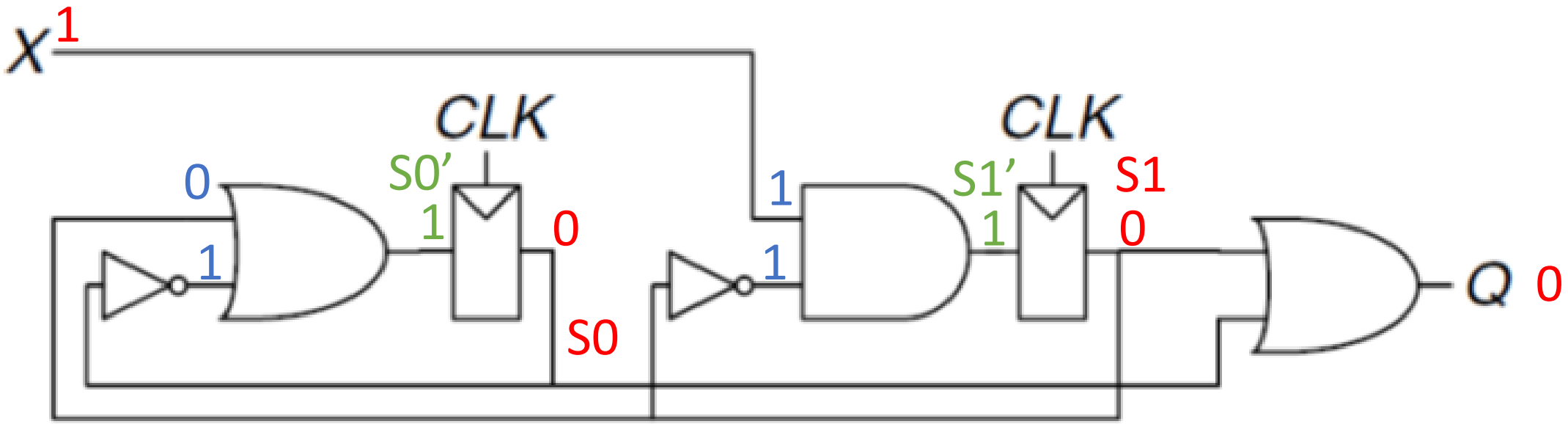
Step By Step Working : S1 = 0, S0 = 0, X=0



current state		input	next state	
s_1	s_0	x	s'_1	s'_0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	X	X	0	1

current state		output
s_1	s_0	q
0	0	0
0	1	1
1	X	1

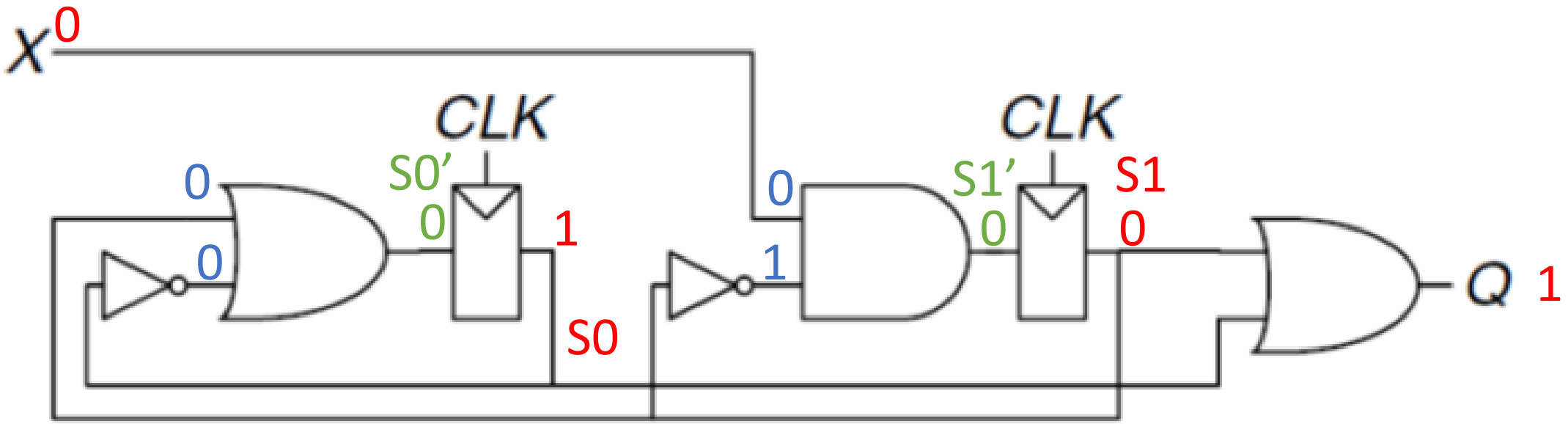
Step By Step Working : S1 = 0, S0 = 0, X=1



current state		input	next state	
s_1	s_0	x	s'_1	s'_0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	X	X	0	1

current state		output
s_1	s_0	q
0	0	0
0	1	1
1	X	1

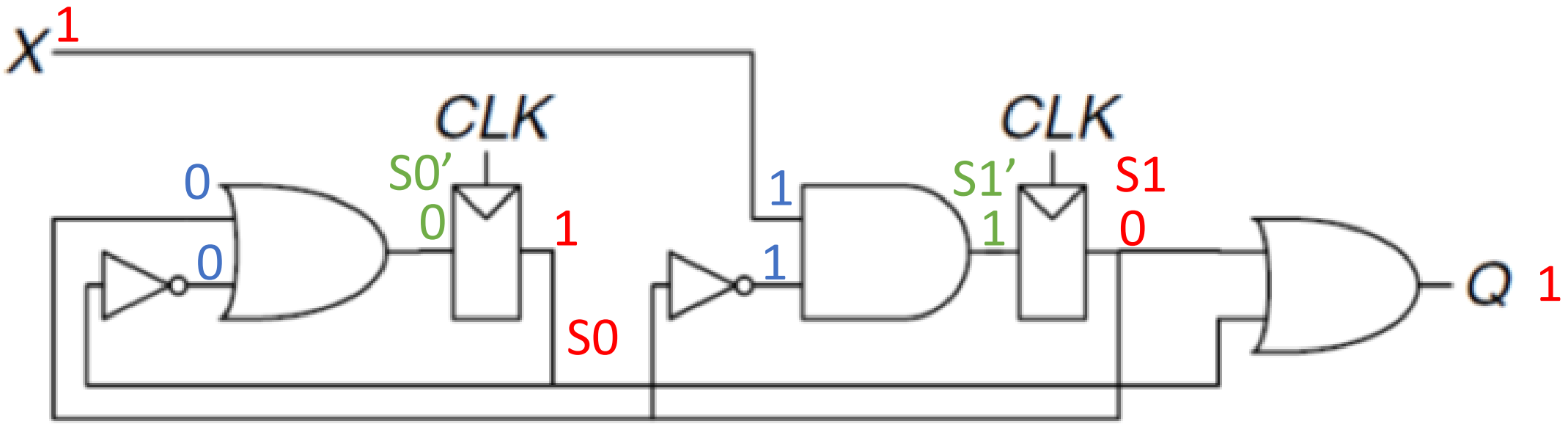
Step By Step Working : S1 = 0, S0 = 1, X=0



current state		input	next state	
s_1	s_0	x	s'_1	s'_0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	X	X	0	1

current state		output
s_1	s_0	q
0	0	0
0	1	1
1	X	1

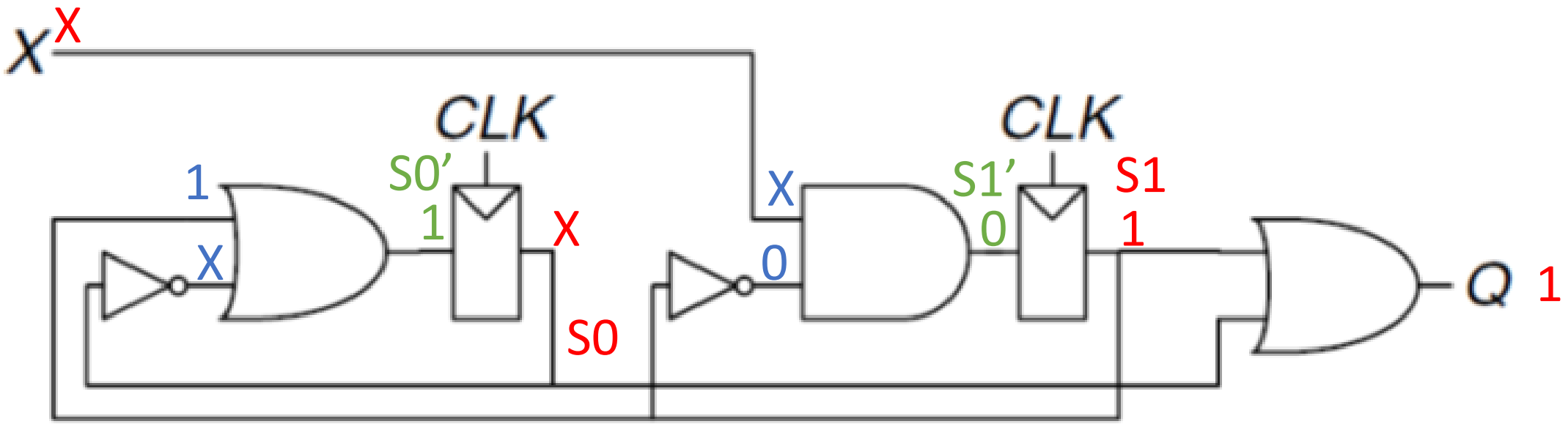
Step By Step Working : S1 = 0, S0 = 1, X=1



current state		input	next state	
s_1	s_0	x	s'_1	s'_0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	X	X	0	1

current state		output
s_1	s_0	q
0	0	0
0	1	1
1	X	1

Step By Step Working : S1 = 1, S0 = X, X=X

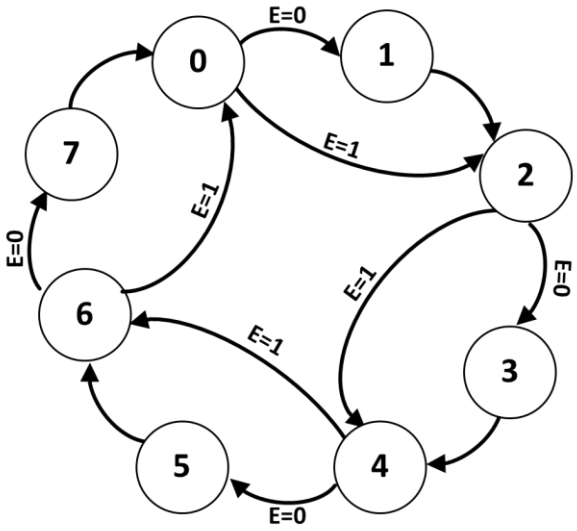


current state		input	next state	
s_1	s_0	x	s'_1	s'_0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	X	X	0	1

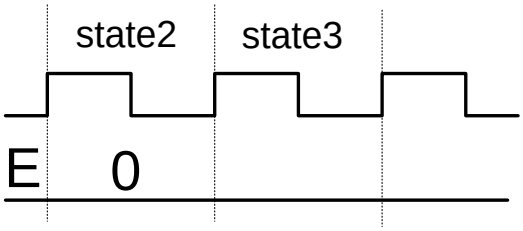
current state		output
s_1	s_0	q
0	0	0
0	1	1
1	X	1

Question 7

(a)



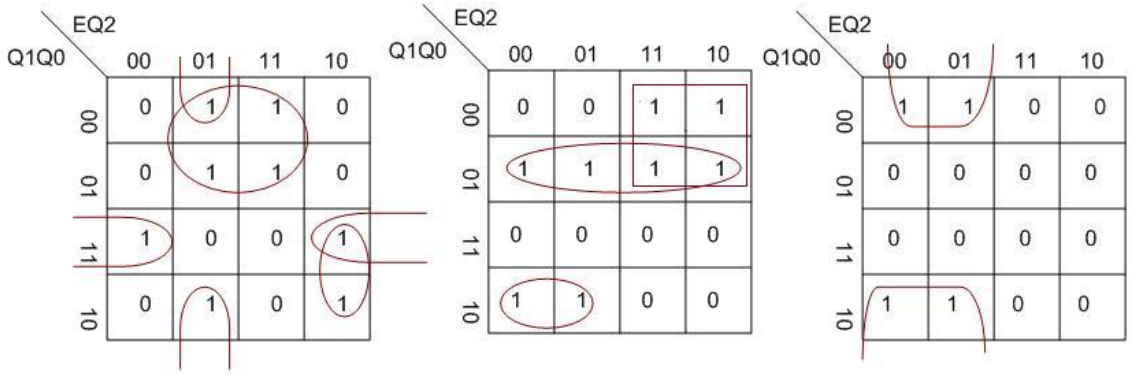
(b) In state 2, if E=0 the next state will be state 3.



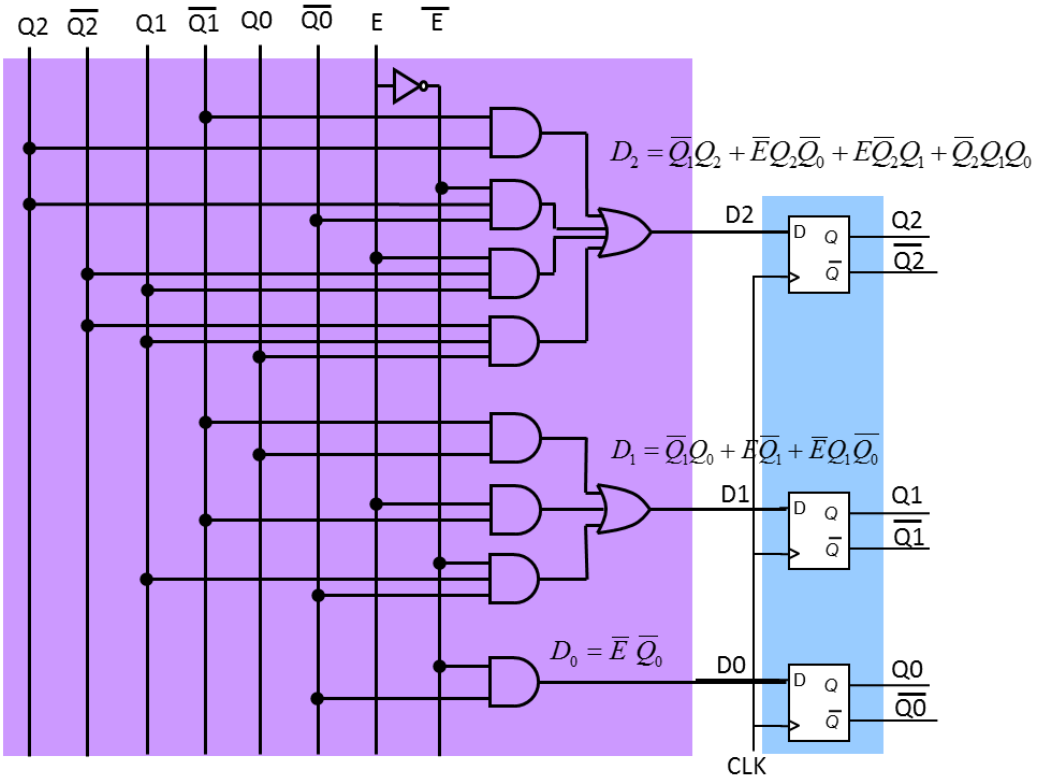
During state 2, the machine checks for the value of E, just before the next clock edge comes. If E=0, this will make the machine go to state 3 in the next clock cycle.

(c)

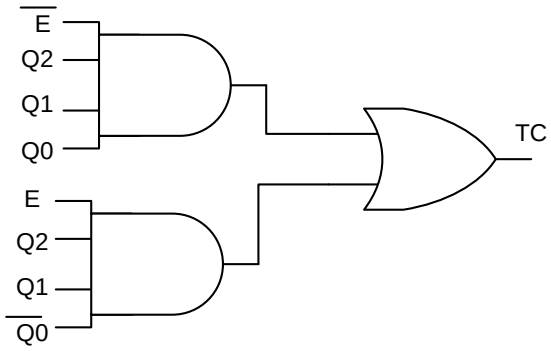
E	Q2	Q1	Q0	Q2+ / D2	Q1+ / D1	Q0+ / D0
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	1
0	0	1	1	1	0	0
0	1	0	0	1	0	1
0	1	0	1	1	1	0
0	1	1	0	1	1	1
0	1	1	1	0	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	0	0	0
1	1	1	1	0	0	0



$$D_2 = \overline{Q}_1 Q_2 + \overline{E} Q_2 \overline{Q}_0 + E \overline{Q}_2 Q_1 + \overline{Q}_2 Q_1 Q_0 \qquad D_1 = \overline{Q}_1 Q_0 + E \overline{Q}_1 + \overline{E} Q_1 \overline{Q}_0 \qquad D_0 = \overline{E}\ \overline{Q}_0$$

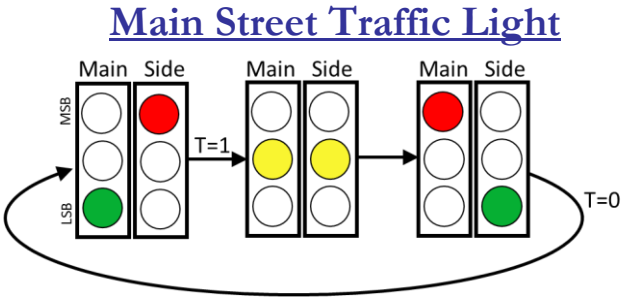


d) TC is TRUE if the state is 7 and EVEN=0, or if the state is 6 and EVEN=1.

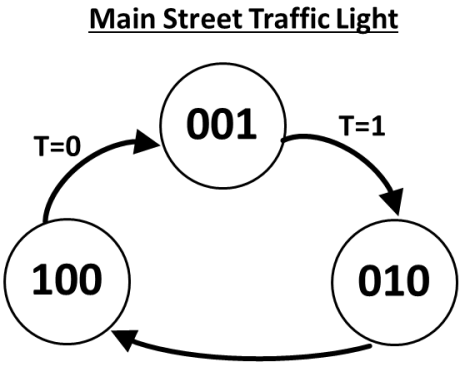


$$TC = \overline{E} Q_2 Q_1 Q_0 + E Q_2 Q_1 \overline{Q}_0$$

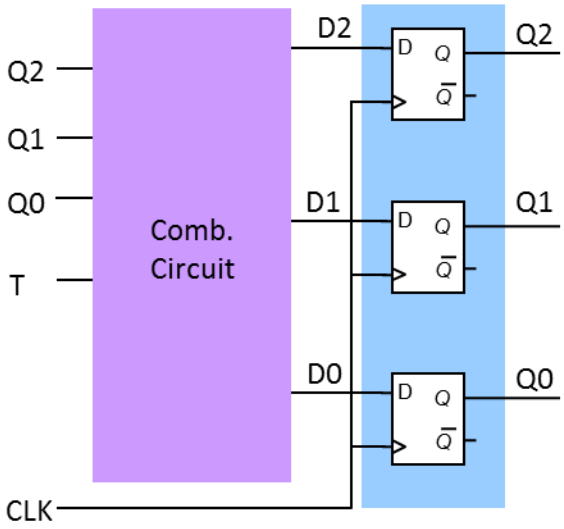
Question 8



1) State Diagram



2) Functional Block Diagram



3) Next State Table → Truth table of the Combinational Circuit

	Current State			Next State		
T	Q2	Q1	Q0	Q2+ = D2	Q1+ = D1	Q0 + = D0
0	0	0	1	0	0	1
0	0	1	0	1	0	0
0	1	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	1	0	0	1	0	0
X	Other States			X	X	X

4) Realize the Circuit

D2 Kmap

Q2Q1 \ Q0 T	00	01	11	10
00	X	X	0	0
01	1	1	X	X
11	X	X	X	X
10	0	1	X	X

$D_2 = \overline{Q_0}T + Q_1$

D1 Kmap

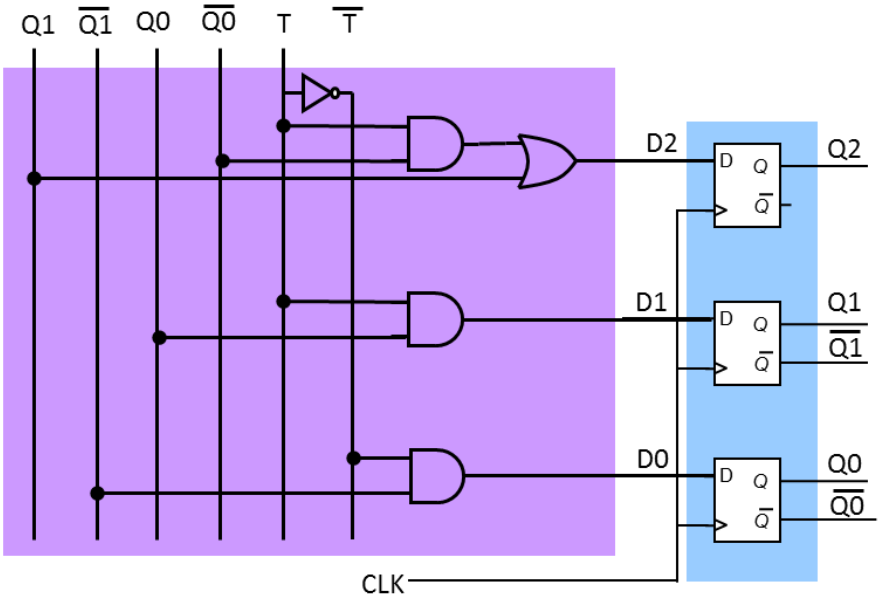
Q2Q1 \ Q0 T	00	01	11	10
00	X	X	1	0
01	0	0	X	X
11	X	X	X	X
10	0	0	X	X

$D_1 = Q_0T$

D0 Kmap

Q2Q1 \ Q0 T	00	01	11	10
00	X	X	0	1
01	0	0	X	X
11	X	X	X	X
10	1	0	X	X

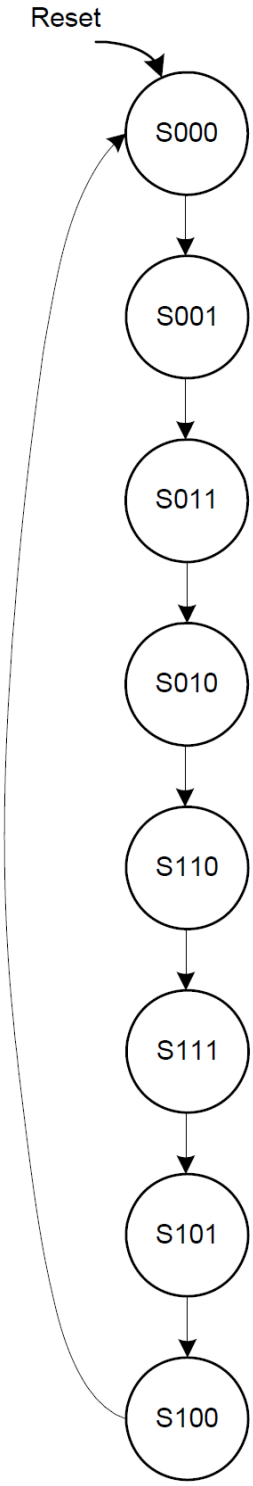
$D_0 = \overline{T}\overline{Q_1}$



This question can alternatively be solved by the FSM approach.

Question 9

State Transition Diagram



Next State Table

current state $s_{2:0}$	next state $s'_{2:0}$
000	001
001	011
011	010
010	110
110	111
111	101
101	100
100	000

$$S'_2 = S_1\overline{S_0} + S_2S_0$$

$$S'_1 = \overline{S_2}S_0 + S_1\overline{S_0}$$

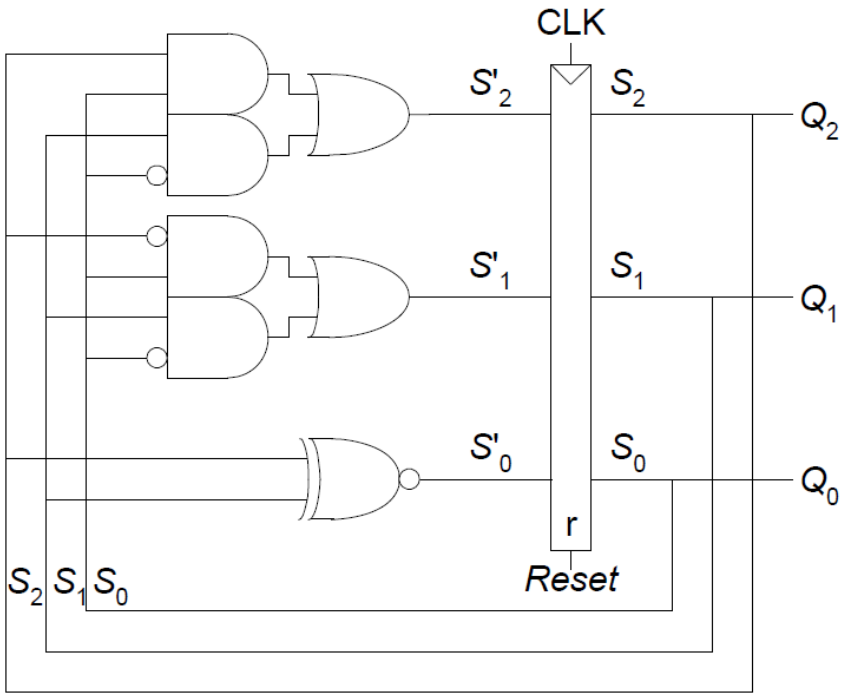
$$S'_0 = \overline{S_2 \oplus S_1}$$

$$Q_2 = S_2$$

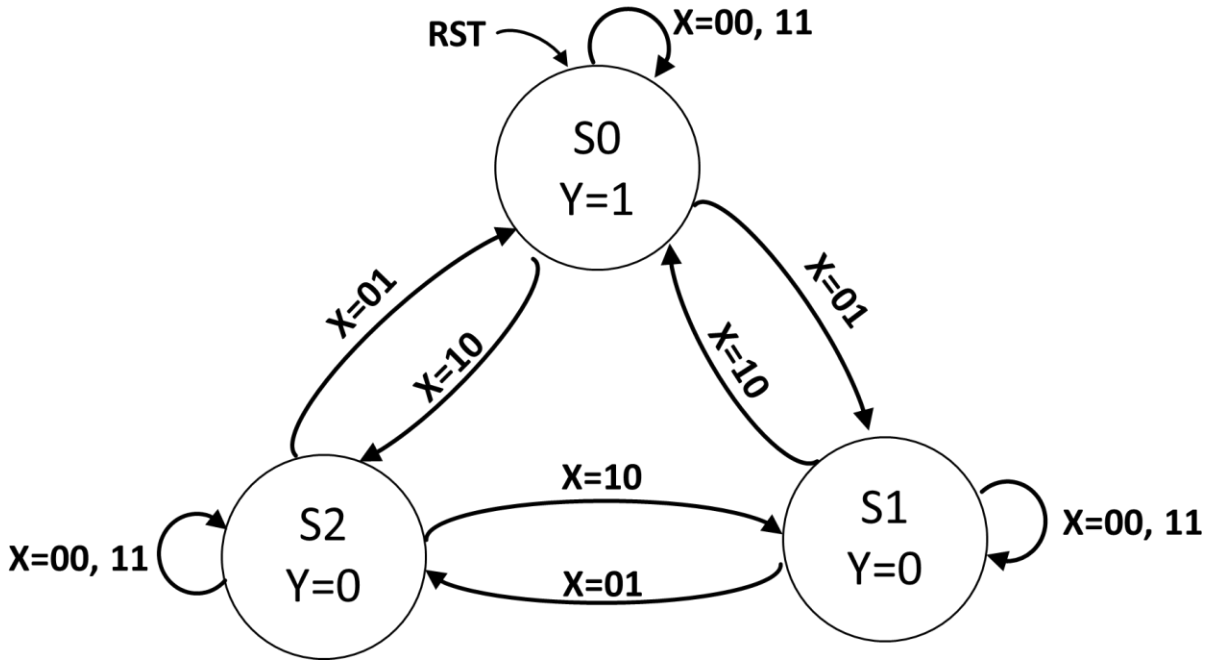
$$Q_1 = S_1$$

$$Q_0 = S_0$$

Final Circuit Implementation



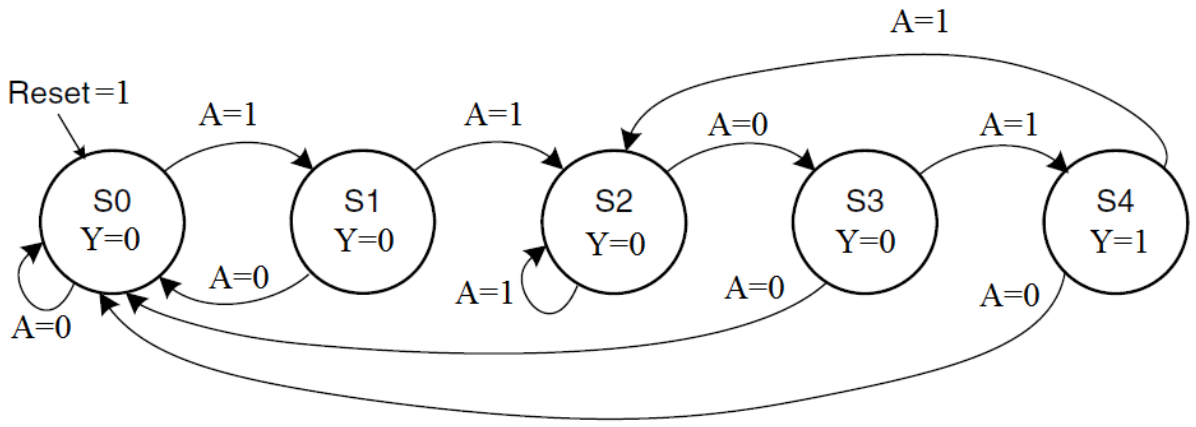
Question 10



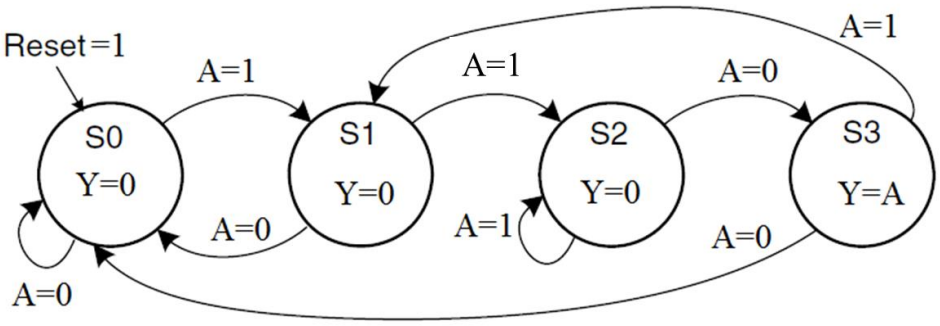
In State S0 : the cumulative sum is a multiple of 3 (3n),
State S1 : the cumulative sum is a multiple of 3, plus 1 (3n + 1)
State S2 : the cumulative sum is a multiple of 3, plus 2 (3n + 2)

Question 11

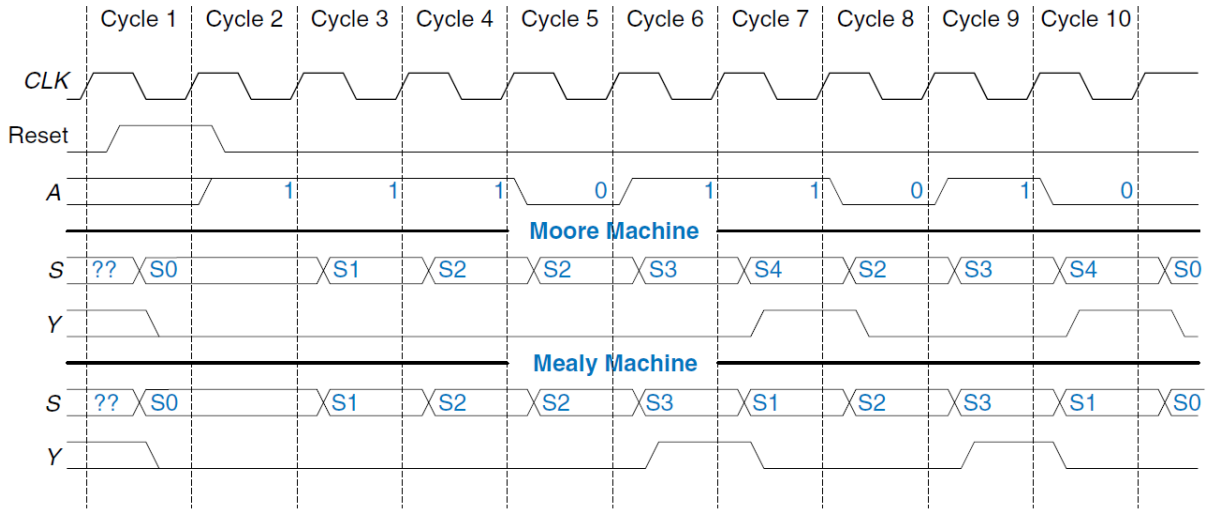
For a more detailed explanation, please refer to the subsequent pages.



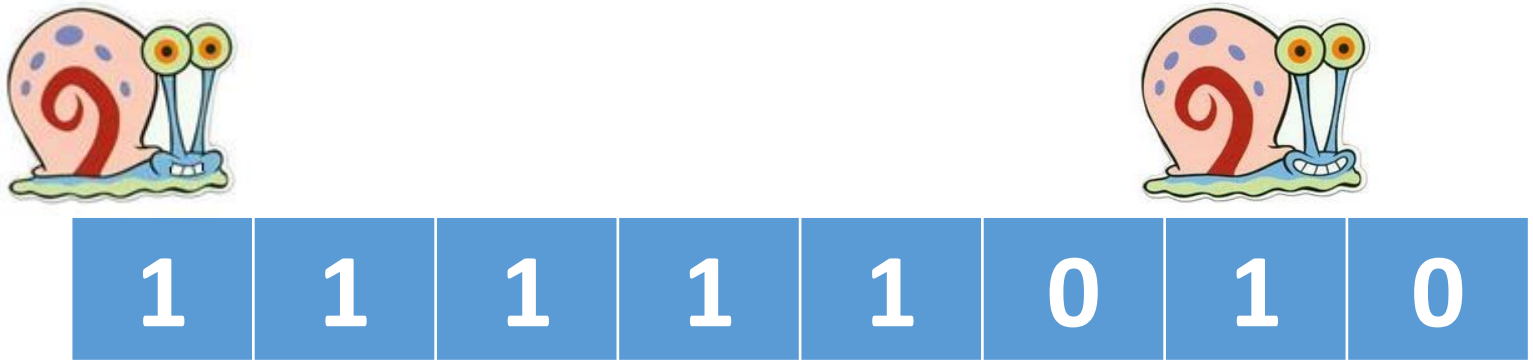
Mealy :



The Moore machine requires five states, while in comparison, the Mealy machine requires only four states. An easy way to remember the difference is that a Moore machine typically has *More* states for a given problem.

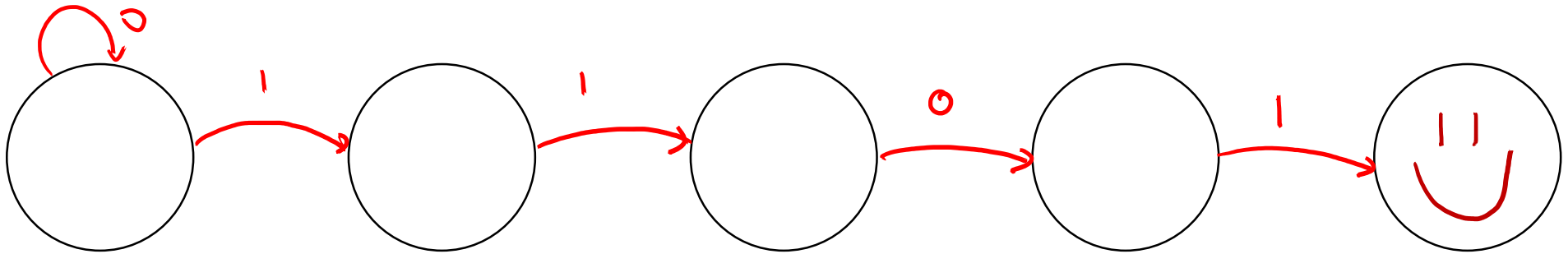


EE2026 Extra Practice Question Set : Question 9

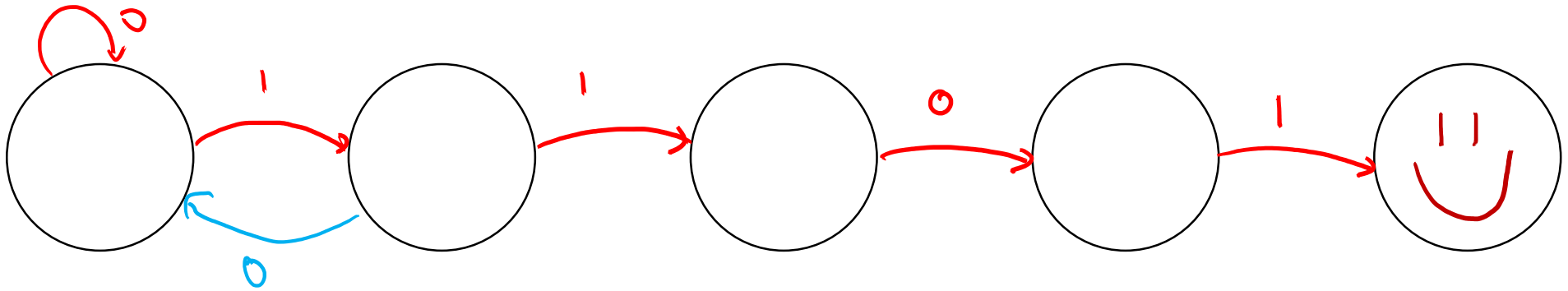


Alyssa owns a pet robotic snail with an FSM brain. The snail crawls from left to right along a paper tape containing a sequence of 1's and 0's. On each clock cycle, the snail crawls to the next bit. The snail smiles when the last four bits that it has crawled over are, from left to right, 1101.

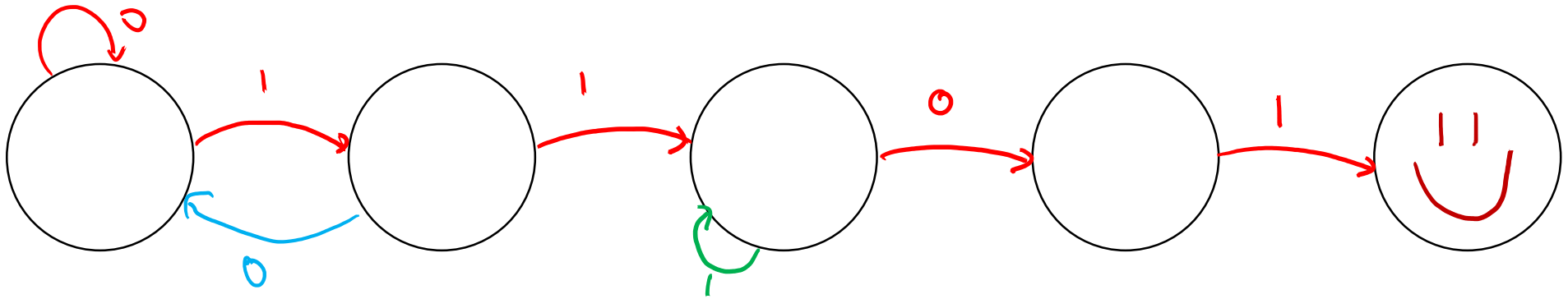
Detecting …0 0 0 1 1 0 1…



Detecting …10101010…



Detecting …11111101…



Detecting ...11111100...

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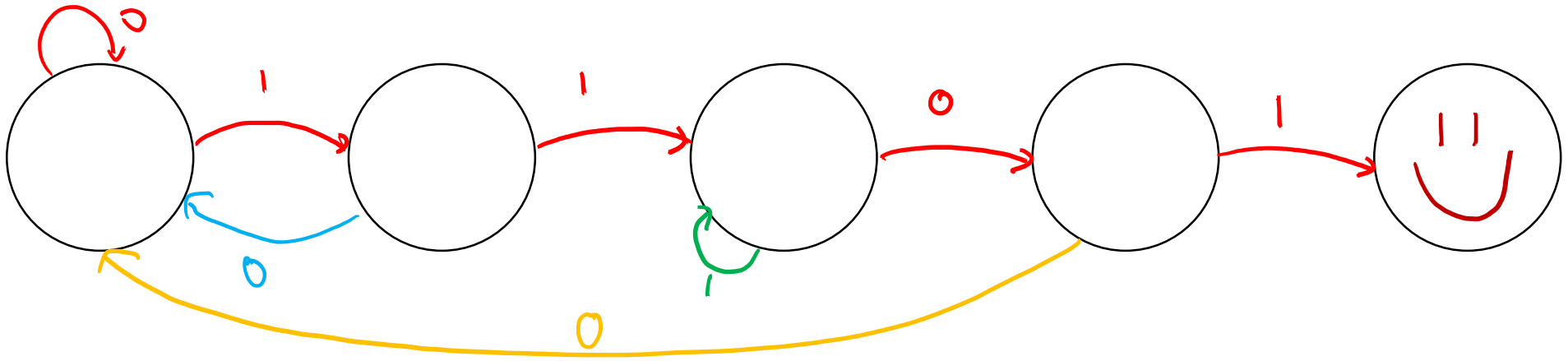
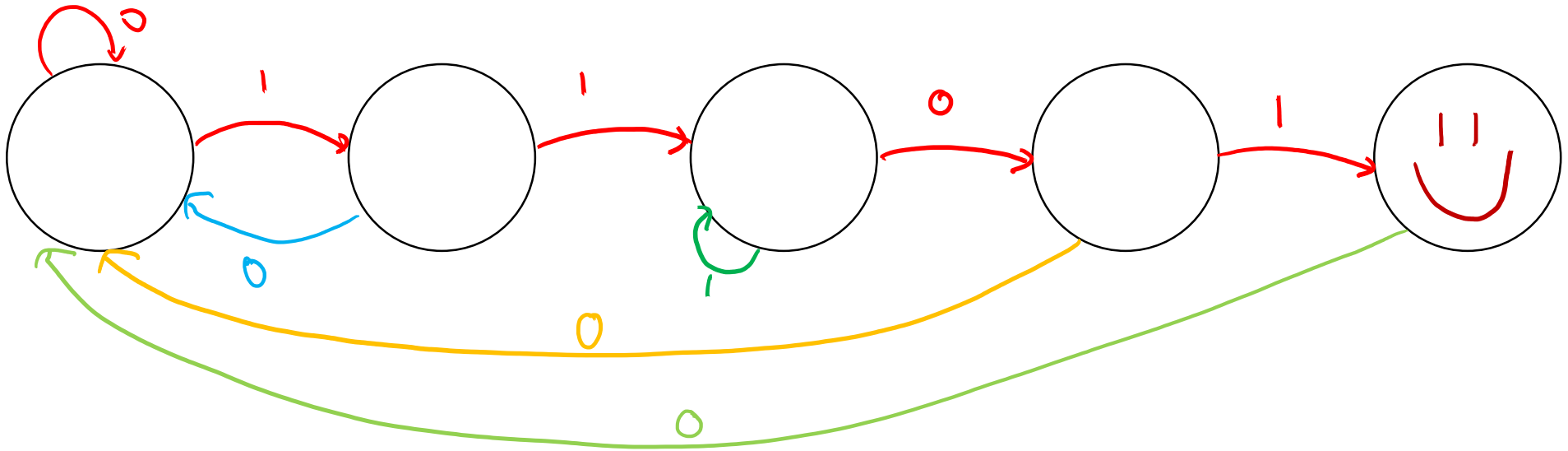
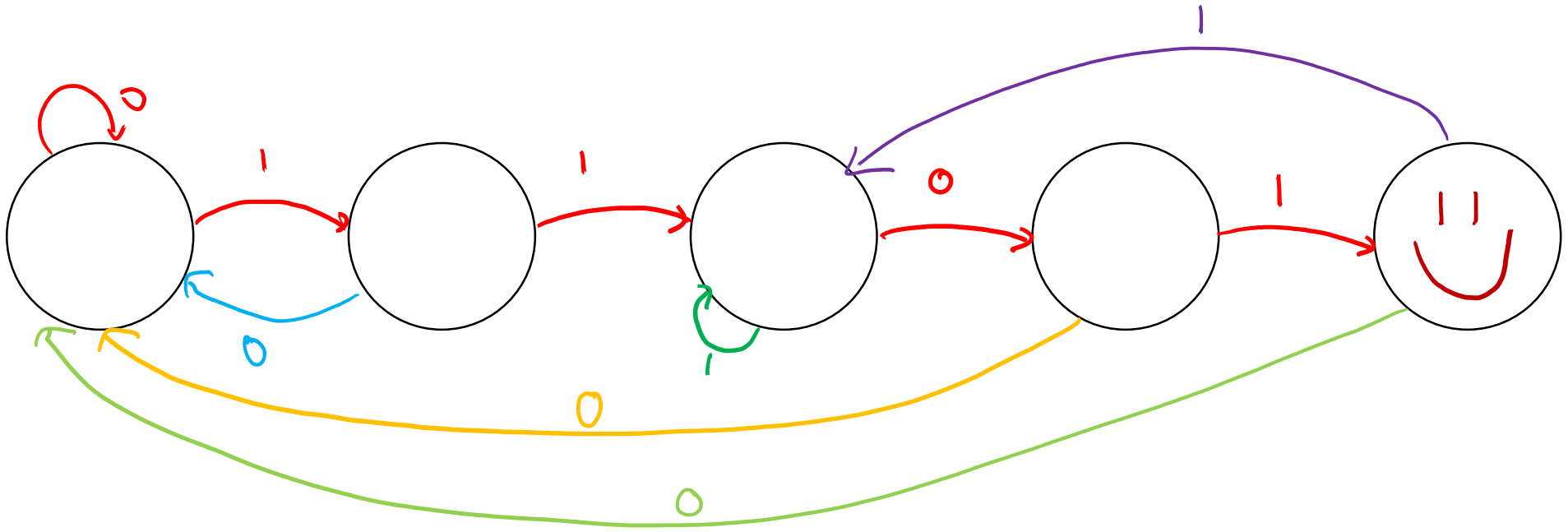


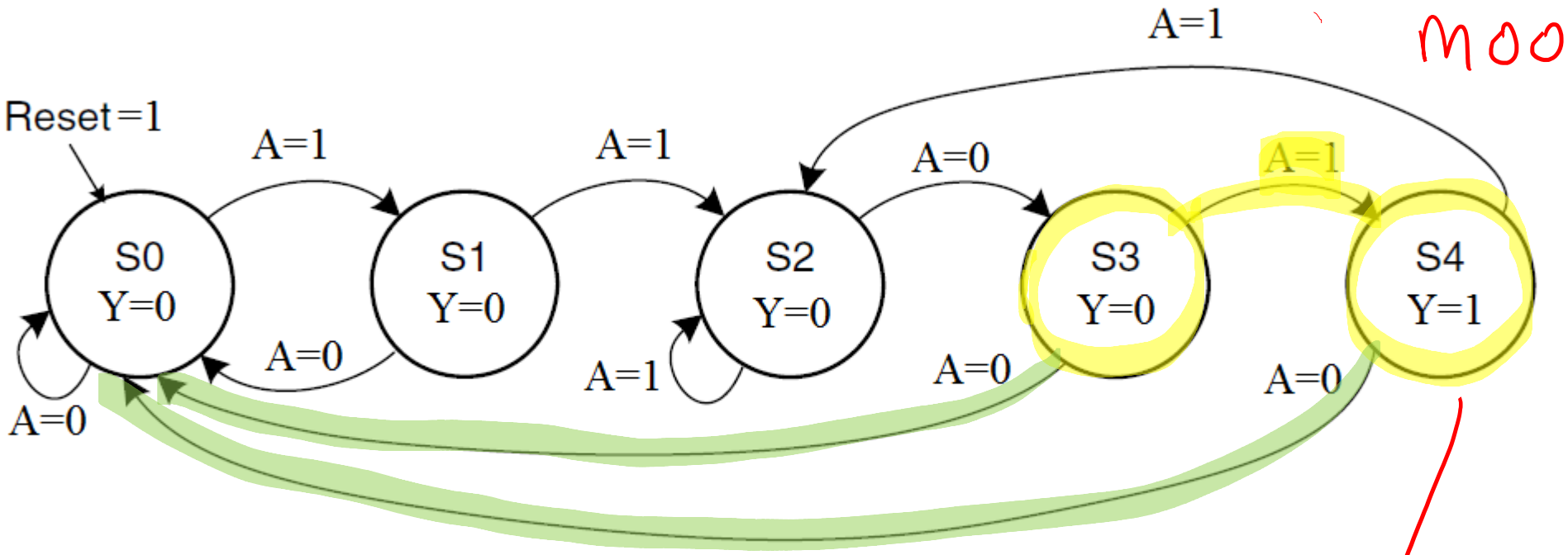
Detecting ... 0011010...

reset



Detecting ... 1111101101101 ...

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A=1
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Y=0
S1
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S2
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S3
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S4
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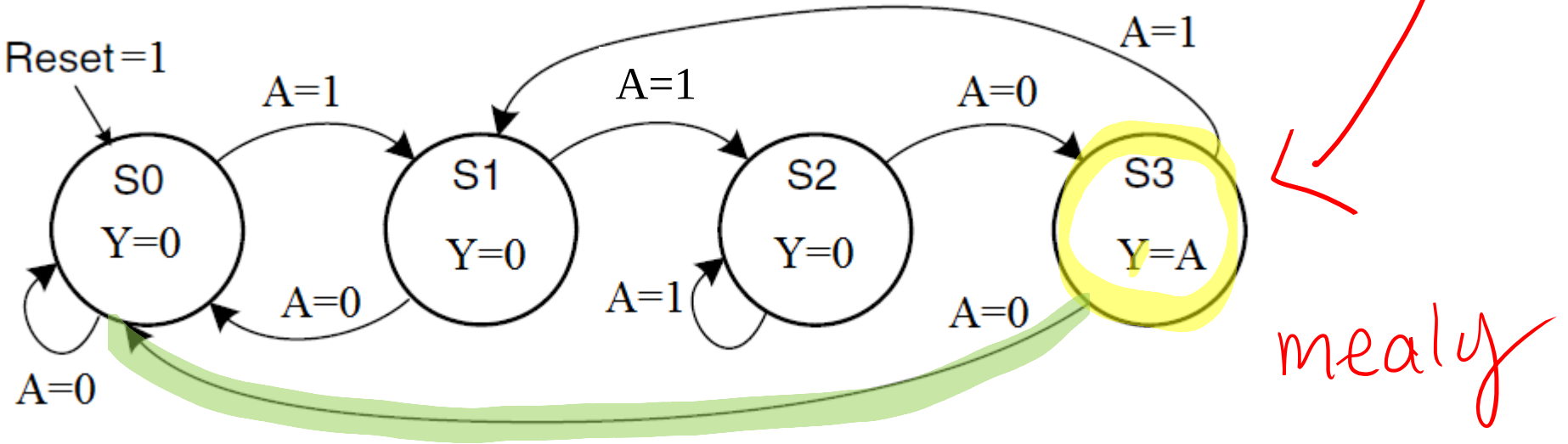
moore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mealy